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10/698,620	11/01/2003	Fusao Ishii	FIshii001	9893

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EXAMINER	
THOMAS, BRANDI N	

ART UNIT	PAPER NUMBER
2873	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/698,620	ISHII, FUSAO	
	Examiner	Art Unit	
	Brandi N Thomas	2873	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/1/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Detailed Action*.

DETAILED ACTION

Information Disclosure Statement

1. Acknowledgement is made of receipt of Information Disclosure Statement(s) (PTO-1449) filed 11/1/03. An initialed copy is attached to this Office Action.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-51 are rejected under 35 U.S.C. 102(e) as being anticipated by Patel et al. (US 2004/0125347).

Regarding claim 1, Patel et al. discloses, in figures 2 and 3A, an electromechanical micromirror device (200), comprising: a device substrate (202) with a lst surface and a 2nd surface; control circuitry (not shown, figure 2 shows the 2nd surface of the device substrate) disposed on said lst surface of said substrate, and a micromirror section (215) disposed on said 2nd surface of said substrate, wherein said micromirror section (215) comprises: a micromirror (201), and at least 1 support structure (230) for supporting said micromirror (201) (sections 0047 and 0048).

Regarding claim 2, Patel et al. discloses, in figures 2 and 3A, an electromechanical micromirror device (200), wherein said control circuitry is selected from the group consisting of: CMOS circuits, NMOS circuits, PMOS circuits, bipolar circuits, BiCMOS circuits, DMOS circuits, HEMT circuits, amorphous silicon thin film transistor circuits, polysilicon thin film transistor circuits, SiGe transistor circuits, SiC transistor circuits, GaN transistor circuits, GaAs transistor circuits, InP transistor circuits, CdSe transistor circuits, organic transistor circuits, and conjugated polymer transistor circuits (section 0043).

Regarding claim 3, Patel et al. discloses, in figures 2 and 3A, an electromechanical micromirror device (200), wherein said device substrate (201) is selected from the group consisting of silicon-on-insulator (SOI), silicon, polycrystalline silicon, glass, plastic, ceramic, germanium, SiGe, SiC, sapphire, quartz, GaAs, and InP (sections 0043 and 0047).

Regarding claim 4, Patel et al. discloses, in figures 2, 3A, and 4C, an electromechanical micromirror device (200), wherein said micromirror section (215) additionally comprises at least 1 addressing electrode (283) for actuating said micromirror (201) (section 0047).

Regarding claim 5, Patel et al. discloses, in figures 2, 3A, and 3C, an electromechanical micromirror device (200), additionally comprising at least 1 electrically conductive routing line (213) integral with said device substrate (202) that connects said control circuitry to said at least 1 addressing electrode (283) (section 0049).

Regarding claim 6, Patel et al. discloses, in figures 2, 3, and 4C, an electromechanical micromirror device (200), wherein said at least 1 electrically conductive routing line

(213)comprises a via through said substrate (202) and a metallization in said via (sections 0047 and 0049).

Regarding claim 7, Patel et al. discloses, in figure 6B, an electromechanical micromirror device (200), wherein said device substrate (202) additionally comprises an insulating layer (301 and 307) between said lst surface and said 2nd surface (section 0069).

Regarding claim 8, Patel et al. discloses, in figures 2 and 3A-3C, an electromechanical micromirror device (200), wherein said micromirror (201) is a metallic mirror (section 0058).

Regarding claim 9, Patel et al. discloses, in figures 2 and 3A-3C, an electromechanical micromirror device (200), wherein said micromirror (201) is a multilayer dielectric mirror (section 0058).

Regarding claim 10, Patel et al. discloses, in figures 2 and 3A-3C, an electromechanical micromirror device (200), wherein the reflective side (210) of said micromirror (201) is substantially planar with neither recesses nor protrusions (figure 2).

Regarding claim 11, Patel et al. discloses, in figures 2-6B, an electromechanical micromirror device (200), wherein the reflective surface (210) of said micromirror (201) has no edges that are perpendicular to the projection of the incident light propagation vector onto the plane of said device substrate (202) (section 0012) (figures 2-6).

Regarding claim 12, Patel et al. discloses, in figure 2, an electromechanical micromirror device (200), wherein said reflective surface (210) of said micromirror (201) is in the shape of a polygon (section 0049).

Regarding claim 13, Patel et al. discloses, in figure 2, an electromechanical micromirror device (200), wherein said polygon is selected from the group consisting of a rectangle and a hexagon (section 0049).

Regarding claim 14, Patel et al. discloses, in figures 2, 3A, and 3B, an electromechanical micromirror device (200), wherein said micromirror section additionally comprises: a torsion hinge (230) that is disposed to support said micromirror support structure (215), and a pair of support structures (251) for said torsion hinge (230) that supports said torsion hinge (230) on said substrate (201) (sections 0048 and 0050).

Regarding claim 15, Patel et al. discloses, in figures 2, 3A, and 3B, an electromechanical micromirror device (200), wherein said micromirror section (215) additionally comprises at least 1 stopping member (255) that limits the rotation of said micromirror (201) (section 0050).

Regarding claim 16, Patel et al. discloses, in figures 2, 3A, and 3B, an electromechanical micromirror device (200), wherein said at least 1 stopping member (255) comprises: a lst stopping member (255), a that limits the rotation of said micromirror (201) in a lst direction, and a 2nd stopping member (255) that limits the rotation of said micromirror in a direction opposite to said lst direction (section 0050).

Regarding claim 17, Patel et al. discloses, in figures 2 and 3A, an array of electromechanical micromirror device (200),comprising a plurality of electromechanical micromirror devices (200) disposed in a 1-dimensional or 2- dimensional array (section 0053), comprising: a device substrate (202) with a lst surface and a 2nd surface; control circuitry (not shown, figure 2 shows the 2nd surface of the device substrate) disposed on said lst surface of said substrate, and an array micromirror sections (215) disposed on said 2nd surface of said substrate,

wherein said micromirror section (215) comprises: a micromirror (201), and at least 1 support structure (230) for supporting said micromirror (201) (sections 0047 and 0048).

Regarding claim 18, Patel et al. discloses, in figures 2 and 3A, an array of electromechanical micromirror device (200),comprising a plurality of electromechanical micromirror devices (200) disposed in a 1-dimensional or 2- dimensional array (section 0053), wherein said control circuitry is selected from the group consisting of: CMOS circuits, NMOS circuits, PMOS circuits, bipolar circuits, BiCMOS circuits, DMOS circuits, HEMT circuits, amorphous silicon thin film transistor circuits, polysilicon thin film transistor circuits, SiGe transistor circuits, SiC transistor circuits, GaN transistor circuits, GaAs transistor circuits, InP transistor circuits, CdSe transistor circuits, organic transistor circuits, and conjugated polymer transistor circuits (section 0043).

Regarding claim 19, Patel et al. discloses, in figures 2 and 3A, an array of electromechanical micromirror device (200),comprising a plurality of electromechanical micromirror devices (200) disposed in a 1-dimensional or 2- dimensional array (section 0053), wherein said device substrate (201) is selected from the group consisting of silicon-on-insulator (SOI), silicon, polycrystalline silicon, glass, plastic, ceramic, germanium, SiGe, SiC, sapphire, quartz, GaAs, and InP (sections 0043 and 0047).

Regarding claim 20, Patel et al. discloses, in figures 2 and 3A, an array of electromechanical micromirror device (200),comprising a plurality of electromechanical micromirror devices (200) disposed in a 1-dimensional or 2- dimensional array (section 0053), wherein said micromirror section (215) additionally comprises at least 1 addressing electrode (283) for actuating said micromirror (201) (section 0047).

Regarding claim 21, Patel et al. discloses, in figures 2, 3A, and 3C, an array of electromechanical micromirror device (200),comprising a plurality of electromechanical micromirror devices (200) disposed in a 1-dimensional or 2- dimensional array (section 0053), additionally comprising at least 1 electrically conductive routing line (213) integral with said device substrate (202) that connects said control circuitry to said at least 1 addressing electrode (283) (section 0049).

Regarding claim 22, Patel et al. discloses, in figures 2, 3, and 4C, an array of electromechanical micromirror device (200),comprising a plurality of electromechanical micromirror devices (200) disposed in a 1-dimensional or 2- dimensional array (section 0053), an electromechanical micromirror device (200), wherein said at least 1 electrically conductive routing line (213) comprises a via through said substrate (202) and a metallization in said via (sections 0047 and 0049).

Regarding claim 23, Patel et al. discloses, in figure 6B, an array of electromechanical micromirror device (200),comprising a plurality of electromechanical micromirror devices (200) disposed in a 1-dimensional or 2- dimensional array (section 0053), wherein said device substrate (202) additionally comprises an insulating layer (301 and 307) between said lst surface and said 2nd surface (section 0069).

Regarding claim 24, Patel et al. discloses, in figures 2 and 3A-3C, an array of electromechanical micromirror device (200),comprising a plurality of electromechanical micromirror devices (200) disposed in a 1-dimensional or 2- dimensional array (section 0053), wherein said micromirror (201) is a metallic mirror (section 0058).

Regarding claim 25, Patel et al. discloses, in figures 2 and 3A-3C, an array of electromechanical micromirror device (200),comprising a plurality of electromechanical micromirror devices (200) disposed in a 1-dimensional or 2- dimensional array (section 0053), wherein said micromirror (201) is a multilayer dielectric mirror (section 0058).

Regarding claim 26, Patel et al. discloses, in figures 2 and 3A-3C, an array of electromechanical micromirror device (200),comprising a plurality of electromechanical micromirror devices (200) disposed in a 1-dimensional or 2- dimensional array (section 0053), wherein the reflective side (210) of said micromirror (201) is substantially planar with neither recesses nor protrusions (figure 2).

Regarding claim 27, Patel et al. discloses, in figures 2-6B, an array of electromechanical micromirror device (200),comprising a plurality of electromechanical micromirror devices (200) disposed in a 1-dimensional or 2- dimensional array (section 0053), wherein the reflective surface (210) of said micromirror (201) has no edges that are perpendicular to the projection of the incident light propagation vector onto the plane of said device substrate (202) (section 0012) (figures 2-6).

Regarding claim 28, Patel et al. discloses, in figure 2, an array of electromechanical micromirror device (200),comprising a plurality of electromechanical micromirror devices (200) disposed in a 1-dimensional or 2- dimensional array (section 0053), wherein said reflective surface (210) of said micromirror (201) is in the shape of a polygon (section 0049).

Regarding claim 29, Patel et al. discloses, in figure 2, an array of electromechanical micromirror device (200),comprising a plurality of electromechanical micromirror devices (200)

disposed in a 1-dimensional or 2- dimensional array (section 0053), wherein said polygon is selected from the group consisting of a rectangle and a hexagon (section 0049).

Regarding claim 30, Patel et al. discloses, in figures 2, 3A, and 3B, an array of electromechanical micromirror device (200),comprising a plurality of electromechanical micromirror devices (200) disposed in a 1-dimensional or 2- dimensional array (section 0053), wherein said micromirror section additionally comprises: a torsion hinge (230) that is disposed to support said micromirror support structure (215), and a pair of support structures (251) for said torsion hinge (230) that supports said torsion hinge (230) on said substrate (201) (sections 0048 and 0050).

Regarding claim 31, Patel et al. discloses, in figures 2, 3A, and 3B, an array of electromechanical micromirror device (200),comprising a plurality of electromechanical micromirror devices (200) disposed in a 1-dimensional or 2- dimensional array (section 0053), wherein said micromirror section (215) additionally comprises at least 1 stopping member (255) that limits the rotation of said micromirror (201) (section 0050).

Regarding claim 32, Patel et al. discloses, in figures 2, 3A, and 3B, an array of electromechanical micromirror device (200), comprising a plurality of electromechanical micromirror devices (200) disposed in a 1-dimensional or 2- dimensional array (section 0053), wherein said at least 1 stopping member (255) comprises: a lst stopping member (255), a that limits the rotation of said micromirror (201) in a lst direction, and a 2nd stopping member (255) that limits the rotation of said micromirror in a direction opposite to said lst direction (section 0050).

Regarding claim 32, Patel et al. discloses, in figures 2, 3A, and 3B, a spatial light modulator (SLM) comprising an array (section 0045).

Regarding claim 34, Patel et al. discloses, in figures 2 and 3A, a method of fabricating an array of electromechanical micromirror devices (200), comprising the steps of: providing a device substrate (202) with a lst surface and a 2nd surface; forming control circuitry (not shown, figure 2 shows the 2nd surface of the device substrate) on said lst surface of said substrate, and forming a plurality of micromirror sections (215) on said 2nd surface of said substrate, comprising the steps of: forming a plurality of support structures (230) for supporting the micromirrors (201) , and forming a plurality of micromirrors (201) such that each said micromirror (201) is supported by at least 1 said support structure (230) (sections 0047 and 0048).

Regarding claim 35, Patel et al. discloses, in figures 2 and 3A, a method of fabricating an array of electromechanical micromirror devices (200), wherein said step of forming control circuitry (not shown, figure 2 shows the 2nd surface of the device substrate) comprises a step of fabricating circuits selected from the group consisting of: CMOS circuits, NMOS circuits, PMOS circuits, bipolar transistor circuits, BiCMOS circuits, DMOS circuits, HEMT circuits, amorphous silicon thin film transistor circuits, polysilicon thin film transistor circuits, SiGe transistor circuits, SiC transistor circuits, GaN transistor circuits, GaAs transistor circuits, InP transistor circuits, CdSe transistor circuits, organic transistor circuits, and conjugated polymer transistor circuits (section 0043).

Regarding claim 36, Patel et al. discloses, in figures 2 and 3A, a method of fabricating an array of electromechanical micromirror devices (200), wherein said device substrate (201) is

selected from the group consisting of silicon-on-insulator (SOI), silicon, polycrystalline silicon, glass, plastic, ceramic, germanium, SiGe, SiC, sapphire, quartz, GaAs, and InP (sections 0043 and 0047).

Regarding claim 37, Patel et al. discloses, in figures 2, 3A, and 4C, a method of fabricating an array of electromechanical micromirror devices (200), wherein said step of forming said micromirror sections additionally comprises a step of forming a plurality of addressing electrodes (283) for actuating said plurality of micromirrors (201) (section 0047).

Regarding claim 38, Patel et al. discloses, in figures 2, 3A, and 3C, a method of fabricating an array of electromechanical micromirror devices (200), additionally comprising a step of forming a plurality of electrically conductive routing lines (213) integral with said device substrate (202) that connects said control circuitry (not shown, figure 2 shows the 2nd surface of the device substrate) to said plurality of addressing electrodes (283).

Regarding claim 39, Patel et al. discloses, in figures 2, 3, and 4C, a method of fabricating an array of electromechanical micromirror devices (200), wherein said step of forming said plurality of electrically conductive routing lines (213) comprises the steps of: forming at least 1 via through said substrate (202), and forming a metallization in said at least 1 via (sections 0047 and 0049).

Regarding claim 40, Patel et al. discloses, in figure 6B, a method of fabricating an array of electromechanical micromirror devices (200), wherein said device substrate (202) additionally comprises an insulating layer (301 and 307) between said lst surface and said 2nd surface (section 0069).

Regarding claim 41, Patel et al. discloses, in figures 2 and 3A-3C, a method of fabricating an array of electromechanical micromirror devices (200), wherein said step of forming a plurality of micromirrors (201) comprises a step of forming a reflective metallic coating (210) (section 0058).

Regarding claim 42, Patel et al. discloses, in figures 2 and 3A-3C, a method of fabricating an array of electromechanical micromirror devices (200), wherein said step of forming a plurality of micromirrors (201) comprises a step of forming a reflective multilayer dielectric coating (210) (section 0058).

Regarding claim 43, Patel et al. discloses, in figures 5B and 5C, a method of fabricating an array of electromechanical micromirror devices (200), wherein said step of forming said micromirror sections comprises the steps of: forming said plurality of micromirror support structures (230) such that it is embedded in a layer of sacrificial material (sections 0011, 0013, and 0062), planarizing said layer such that said sacrificial layer and the top of said micromirror support structures (230) are substantially planar (figure 5B), depositing a micromirror material on said planar surface (section 0062); patterning said micromirror material to form a plurality of micromirrors (section 0068), and removing said sacrificial layer by an etching process (section 0063 and 0068).

Regarding claim 44, Patel et al. discloses, in figures 5B and 5C, a method of fabricating an array of electromechanical micromirror devices (200), wherein said sacrificial layer material is selected from the group consisting of photoresist polymer, silicon oxide, silicon nitride, silicon oxynitride, and amorphous silicon (section 0062).

Regarding claim 45, Patel et al. discloses, in figures 5B and 5C, a method of fabricating an array of electromechanical micromirror devices (200), wherein said planarizing step comprises a chemical mechanical polishing (CMP) process (section 0062).

Regarding claim 46, Patel et al. discloses, in figures 2-6B, a method of fabricating an array of electromechanical micromirror devices (200), wherein said step of forming a plurality of micromirrors (201) comprises a step of patterning said micromirrors to have no edges that are perpendicular to the projection of the incident light propagation vector onto the plane of said device substrate (202) (section 0012) (figures 2-6).

Regarding claim 47, Patel et al. discloses, in figure 2, a method of fabricating an array of electromechanical micromirror devices (200), wherein each said micromirror is patterned to be in the shape of a polygon (section 0049).

Regarding claim 48, Patel et al. discloses, in figure 2, a method of fabricating an array of electromechanical micromirror devices (200), wherein said polygon is selected from the group consisting of a rectangle and a hexagon (section 0049).

Regarding claim 49, Patel et al. discloses, in figures 5B and 5C, a method of fabricating an array of electromechanical micromirror devices (200), additionally comprising a step of forming a torsion hinge (230) for supporting each said mirror support structure (215), said step comprising: forming a plurality of supports (251) for supporting torsion hinges (230), and forming a plurality of torsion hinges (230) (sections 0048 and 0050).

Regarding claim 50, Patel et al. discloses, in figures 5B and 5C, a method of fabricating an array of electromechanical micromirror devices (200), additionally comprising the step of:

forming at least 1 stopping member (255) that limits the rotation of each said micromirror (201) (section 0050).

Regarding claim 51, Patel et al. discloses, in figures 5B and 5C, a method of fabricating an array of electromechanical micromirror devices (200), wherein said step of forming at least 1 stopping member (255) comprises: forming a lst stopping member (255) that limits the rotation of said micromirror (201) in a lst direction, and forming a 2nd stopping member (255) that limits the rotation of said micromirror (201) in a direction opposite to said lst direction (section 0050).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 52-60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patel et al. (US 2004/0125347) in view of Chiu et al. (6639713 B2).

Regarding claim 52, Patel et al. discloses a method of fabricating an array of electromechanical micromirror devices, comprising the steps of: forming control circuitry (not shown, figure 2 shows the 2nd surface of the device substrate); forming a plurality of micromirror sections (215) on said exposed insulator layer, comprising the steps of: forming a plurality of support structures (230) for supporting micromirrors (201), and forming a plurality of micromirrors (201) such that each said micromirror (201) is supported by at least 1 said support structure (230) (sections 0047 and 0048) except that it does not show providing a silicon-on-

insulator substrate with an epitaxial top silicon layer, an insulator layer, and a bottom silicon layer forming control circuitry on said epitaxial top silicon layer, removing said bottom silicon layer, thereby exposing the insulator layer. Chiu et al. shows that it is known to provide a silicon-on-insulator substrate with an epitaxial top silicon layer (321), an insulator layer (323), and a bottom silicon layer (324) on said epitaxial top silicon layer, removing said bottom silicon layer, thereby exposing the insulator layer for at least partially intercepting a light beam propagating along a beam path (col. 15, lines 51-53 and col. 21, lines 37-52). Therefore it would have been obvious to someone of ordinary skill in the art at the time the invention was made to combine the device of Patel et al. with the silicon-on-insulator substrate of Chiu et al. for the purpose of at least partially intercepting a light beam propagating along a beam path (col. 15, lines 51-53 and col. 21, lines 37-52).

Regarding claim 53, Patel et al. discloses, in figures 6A-6H, a method of fabricating an array of electromechanical micromirror devices, wherein said step of forming control circuitry comprises a step of fabricating circuits selected from the group consisting of: CMOS circuits, NMOS circuits, PMOS circuits, bipolar transistor circuits, BiCMOS circuits, and DMOS circuits (section 0043).

Regarding claim 54, Patel et al. discloses a method of fabricating an array of electromechanical micromirror devices, including a step of removing said bottom silicon layer but does not specifically disclose removing the bottom silicon layer by backgrinding. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the process of backgrinding for the purpose of ensuring the eradication of the silicon layer on the substrate.

Regarding claim 55, Patel et al. discloses, in figures 6A-6H, a method of fabricating an array of electromechanical micromirror devices, wherein said step of removing said bottom silicon layer comprises chemical mechanical polishing (CMP) (section 0062).

Regarding claim 56, Patel et al. discloses, in figures 6A-6H, a method of fabricating an array of electromechanical micromirror devices, wherein said step of forming said micromirror (201) section additionally comprises a step of forming a plurality of addressing electrodes (283) for actuating said plurality of micromirrors (201) (section 0049).

Regarding claim 57, Patel et al. discloses, in figures 2, 3A, and 6A-6H, a method of fabricating an array of electromechanical micromirror devices, additionally comprising a step of forming a plurality of electrically conductive routing lines (213) integral with said device substrate (202) that connects said control circuitry (not shown, figure 2 shows the 2nd surface of the device substrate) to said plurality of addressing electrodes (282 and 283) (section 0048 and 0049).

Regarding claim 58, Patel et al. discloses, in figures 2, 3A, and 6A-6H, a method of fabricating an array of electromechanical micromirror devices, wherein said step of forming said plurality of electrically conductive routing lines (213) comprises the steps of: forming at least 1 via through said substrate (202), and forming a metallization in said at least 1 via (sections 0047 and 0049).

Regarding claim 59, Patel et al. discloses, in figures 5B and 5C, a method of fabricating an array of electromechanical micromirror devices, wherein said step of forming micromirror sections (215) comprises the steps of: forming said plurality of micromirror support structures (230) such that it is embedded in a layer of sacrificial material (sections 0011, 0013, and 0062),

planarizing said layer such that said sacrificial layer and the top of said micromirror support structures (230) are substantially planar (figure 5B), depositing a micromirror material on said planar surface (section 0062); patterning said micromirror material to form a plurality of micromirrors (section 0068), and removing said sacrificial layer by an etching process (section 0063 and 0068).

Regarding claim 60, Patel et al. discloses, in figures 5B and 5C, a method of fabricating an array of electromechanical micromirror devices, wherein said planarizing step comprises chemical mechanical polishing (CMP) (section 0062).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Patel et al. (US 2004/0008402 A1) discloses a micromirror device along with a method of making such a micromirror device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brandi N Thomas whose telephone number is 571-272-2341. The examiner can normally be reached on 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Georgia Epps can be reached on 571-272-2328. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BNT

BNT
October 21, 2004

Georgia Epps
Supervisory Patent Examiner
Technology Center 2800